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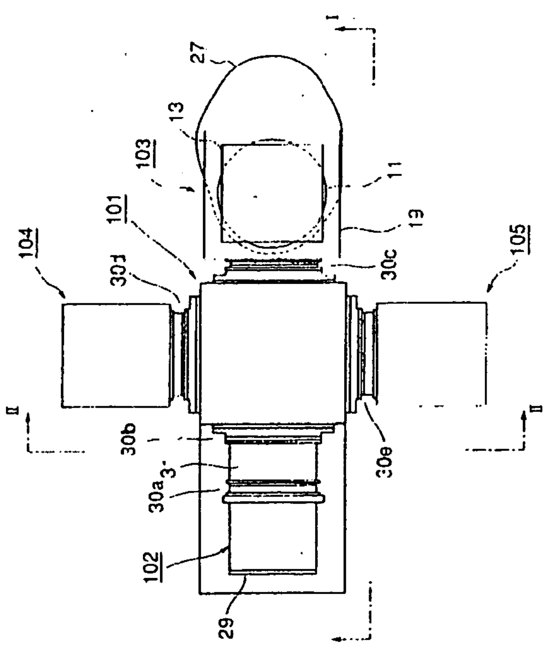
(54) Plasma doping system and plasma doping method

(57) The present invention relates to a plasma doping system capable of dealing with larger-diameter wafers and of introducing impurities to a shallow depth with a lower energy level. The plasma doping system comprises a plasma generation chamber (11) provided with a high-frequency power source (14) for supplying a high-frequency electric power and with antennas (12) for discharging the high-frequency electric power, the plasma generation chamber (11) generating a helicon plasma of a gas containing conduction type imparting impurities by the high-frequency electric power discharged from the antennas (12), an impurity introduction chamber (19) provided with a substrate holding fixture (20) and for causing the helicon plasma of the conduction type impurity containing gas to come into contact with a semiconductor substrate (100) to thereby introduce the conduction type impurities into the semiconductor substrate (100), and a plasma flow passage/shaping chamber (16) interposed between the plasma generation chamber (11) and the impurity introduction chamber (19) and providing a flow passage through which the helicon plasma flows from the plasma generation chamber (11) to the impurity introduction chamber (19), the plasma flow passage/shaping chamber (16) being provided with magnetic field generation means (17) for generating a magnetic field to restrict the extent of the helicon plasma flowing through the flow passage.

Fig. 1



EP 1 054 433 A1

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a plasma doping system and a plasma doping method capable of dealing with larger-diameter wafers and of introducing impurities to a shallow depth with a lower energy level.

2. Description of the Related Art

[0002] In recent fabrication of ultra-high density semiconductor IC devices, one of essential techniques determining main characteristics of transistors or other components is an impurity introduction technique for introducing conduction type imparting impurities (hereinafter, may be referred to simply as impurities) into semiconductor substrates. It is indispensable for the impurity introduction technique to provide a high accuracy control of the dose of impurities or to form high density and very shallow impurity introduction regions. Note that the conduction type imparting impurities when introduced into a semiconductor layer serve to impart a conduction type of p-type or n-type to the semiconductor layer in the introduction region as well as to vary the resistance value of the introduction region.

[0003] Conventional impurity introduction methods include a thermal diffusion method and an ion implantation method. Due to its accurate controllability of dosage, the ion implantation method is in particular advantageous to, e.g., the threshold value control of MOS FETs (Metal-Oxide-Semiconductor field effect transistors).

[0004] In the field of the impurity introduction method for forming high density and extremely shallow impurity introduction regions, particular attention is recently being given to a plasma doping method in place of the thermal diffusion method and the ion implantation method since it is suitable for the application to large diameter wafers.

[0005] The plasma doping method ensures a high throughput for the large diameter wafers as well and allows introduction of impurities with a low energy level, e.g., at room temperature.

[0006] Plasma doping systems for effecting such a plasma doping method are known from Japanese Patent Laid-open Pub. Nos. Hei 2-278720, Hei 5-16656, Hei 6-61161, etc.

[0007] Japanese Patent Laid-open Pub. No. Hei 5-16656 discloses an apparatus in which impurity gas plasma is generated between a pair of parallel plate electrodes to thereby perform the introduction of impurities. Japanese Patent Laid-open Pub. Nos. Hei 2-278720 and Hei 6-61161 disclose apparatuses in which impurity gas plasma is generated by ECR (Electron Cyclotron Resonance) method to thereby effect the introduction of impurities.

[0008] A plasma doping method using an ECR/RF plasma source is also disclosed in Semiconductor Integrated Circuit Technology 52th Symposium Transaction, pp. 165 to 170, June 1997.

[0009] In the method of this transaction, an He based B_2H_6 (diborane) gas is transformed into plasma for the introduction of boron into silicon substrates, after which RTA (Rapid Thermal Annealing) is carried out to form p-type diffusion regions having a surface density of approx. 1 x 10^{21} cm^{-3} and a depth of 50 nm.

[0010] In case of selective introduction of impurities into the silicon substrate by use of the plasma doping method, it is necessary to form a resist film having openings corresponding to the impurity introduction regions so as to allow the impurities to be introduced through the openings of the resist film into the silicon substrate, and to thereafter remove the resist film previous to annealing for the activation of the impurities.

[0011] With the increasing wafer diameters, however, the conventional plasma doping apparatus using ECR method has to be provided with an enlarged plasma generation chamber and impurity introduction chamber and have an enhanced power supply ability. For this reason, the overall dimensions are increased of the system including the ECR plasma source, i.e., a wave guide for micro waves, electromagnets and a matching unit, resulting in an increased floor area required for the placement of the plasma doping system itself.

[0012] In view of the system as a whole required for the introduction of impurities, there is a need for an ashing apparatus to remove the resist film acting as a mask and for an annealer, which will necessitate a further increased floor area for the placement of the system.

SUMMARY OF THE INVENTION

[0013] It is therefore the object of the present invention to provide a plasma doping system and a plasma doping method using the system, capable of reducing the floor areas required for the placement of the plasma doping system itself or for the placement of a plurality of apparatuses for a series of process steps attendant on the plasma doping.

[0014] A plasma doping system of the present invention is provided with a high-frequency power source for generating a helicon plasma of a gas containing conduction type impurities and antennas for discharging the high-frequency electric power.

[0015] By the way, in the event of larger wafer diameters, it is necessary for a plasma doping system using ECR method for the generation of plasma to have a power source providing as very high a frequency as 2.45 GHz or to enlarge the matching unit or the wave guides. In addition, the electromagnets for generating ECR must also be increased in size.

[0016] On the contrary, the system of the present invention is allowed to use a lower frequency as of 13.56

MHz for the high-frequency power source, thereby eliminating the need to increase the size of the high-frequency power source to a large extent. Due to the simple structure, the antennas need not be much enlarged either. In view of its applications, compact ones such as permanent magnets can be used as the magnetic field generation means disposed in the plasma flow passage/ shaping chamber providing the plasma flow passage, thereby enabling the increase in size to be suppressed.

[0017] It is therefore possible for the doping system using the helicon plasma in accordance with the present invention to reduce the floor areas required for the placement of the system as compared with the conventional doping system using the ECR plasma.

[0018] Furthermore, communications are established via a single transfer chamber among the impurity introduction chamber, the ashing chamber and the annealing chamber of the plasma doping system, whereby a single system can perform a series of process steps attendant on the plasma doping such as introduction of conduction type impurities, removal of the resist mask for the selective introduction of the conduction type impurities and activation of the conduction type impurities.

[0019] By the way, in cases where separate apparatuses are used for different steps and individually placed, each apparatus requires a working space for the workers in addition to the net floor area for the space of placement of each apparatus. Those apparatuses may be integrated into a single system such that conveyance robots carry the semiconductor substrate between the different chambers of the system, thereby achieving a reduction in the working space thereof. It is therefore possible to reduce the floor area necessary for the placement of the system in its entirety, as compared with the case of individual placement of each apparatus.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020]

Fig. 1 is a top plan view showing the configuration of a plasma doping system in accordance with an embodiment of the present invention;

Fig. 2 is a cross-sectional view taken along a line I-I of Fig. 1 and viewed from the direction of the arrow;

Fig. 3 is a cross-sectional view taken along a line II-II of Fig. 1 and viewed from the direction of the arrow;

Fig. 4 is a side view showing the configuration of a substrate holding fixture disposed in the plasma doping system in accordance with the embodiment of the present invention;

Fig. 5 is a top plan view showing the array of permanent magnets disposed on the outer periphery of a plasma flow passage/shaping chamber of Fig. 1;

Fig. 6 is a sectional view of the plasma flow passage/shaping chamber of Fig. 1, with a graphic representation of a distribution in section of a magnetic field which is generated within the plasma shaping chamber by the permanent magnets disposed on the outer periphery of the plasma flow passage/ shaping chamber;

Fig. 7 is a side view schematically showing a distribution of a plasma existing within the plasma flow passage/ shaping chamber of Fig. 1;

Fig. 8 is a graphic representation showing a distribution of a plasma existing within the plasma flow passage/ shaping chamber of Fig. 1;

and

Figs. 9A to 9D are cross-sectional views showing a plasma doping method using the plasma doping system in accordance with the embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] The present invention will now be described with reference to the accompanying drawings which illustrate preferred embodiments of the present invention in a non-limitative manner.

[0022] Fig. 1 is a top plan view showing the configuration of a plasma doping system in accordance with an embodiment of the present invention. Fig. 2 is a cross-sectional view taken along a line I-I of Fig. 1 and viewed from the direction of its arrow, and Fig. 3 is a cross-sectional view taken along a ling II-II of Fig. 1 and viewed from the direction of its arrow.

[0023] As can be seen in Figs. 1 to 3, the plasma doping system comprises a transfer chamber 101 in the shape of a rectangular box having four side walls, the inner pressure of which can be reduced. And to each of four side walls are separately connected a load-lock chamber 102 whose inner pressure can be reduced, a plasma doping chamber 103 whose inner pressure can be reduced, an ashing chamber (mask removal chamber) 104 whose inner pressure can be reduced, and an annealing chamber 105 whose inner pressure can be reduced.

[0024] The load-lock chamber 102 provides the inlet and outlet for the semiconductor substrate 100 to and from the plasma doping system. The plasma doping chamber 103 provides a region for introducing the conduction type impurities into a semiconductor layer. The ashing chamber 104 provides a region for removing a mask (photosensitive etching-proof mask) in the form of a resist film. The annealing chamber 105 provides a region for raising the temperature of the semiconductor substrate 100 to activate the conduction type impurities introduced into the semiconductor substrate 100.

[0025] The entrance to the load-lock chamber 102 is provided with a gate valve 29 capable of sealing the interior of the chamber 102 from the exterior. The connection between the transfer chamber 101 and the load-lock chamber 102 is provided with a gate valve 30a, a sub-

strate conveyance path 31 and a gate valve 30b intervening between the load-lock chamber 102 and the transfer chamber 101. The other connections between the transfer chamber 101 and the chambers 103, 104 and 105 are merely provided with gate valves 30c, 30d and 30e, respectively. The opening or closing of the gate valves 30a to 30e enables the chambers 101 to 105 to communicate with one another or to be hermetically sealed from one another.

[0026] Exhaust devices are connected individually to the chambers 101 to 105 in order to ensure that the chambers 101 to 105 can separately reduce their respective inner pressures. Referring to Fig. 2, one exhaust device 28 is only visible connected to the plasma doping chamber 103.

[0027] The load-lock chamber 102 provides the inlet when the semiconductor substrate 100 is loaded from the exterior into the plasma doping system or provides the outlet when it is unloaded from the interior of the plasma doping system to the exterior.

[0028] In case the pressure within the chambers 101, 103 to 105 is lower than the atmospheric pressure, the pressure within the load-lock chamber 102 may be reduced upon the loading or unloading of the semiconductor substrate 100 into or from the system whereby the pressure within the load-lock chamber can be adjusted to the pressures within the chambers 101, 103 to 105, or at least to the pressure within the transfer chamber 101.

[0029] The ashing chamber 104 is a chamber in which the resist film is removed after the selective introduction of the conduction type impurities into the semiconductor substrate 100 through openings in the resist film acting as the mask. Oxygen plasma is used herein as an ashing gas. Provided therefor are an oxygen gas inlet and means for transforming oxygen gas into plasma.

[0030] The annealing chamber 105 is a chamber in which heat treatment is performed for activating the conduction type impurities introduced into the semiconductor substrate 100. The annealing chamber 105 is provided with a heater for heating and a laser irradiation mechanism for a rapid thermal annealer (RTA).

[0031] The plasma doping chamber 103 as illustrated in Fig. 2 comprises, in the mentioned order from up stream along the flow of plasma gas, a plasma generation chamber 11, a plasma flow passage/shaping chamber 16, an impurity introduction chamber 19 and the exhaust chamber 28. The plasma doping chamber 103 is connected through the impurity introduction chamber 19 to the transfer chamber 101.

[0032] Description will be made hereinbelow of a detailed configuration of each part of the plasma doping chamber 103.

[0033] The plasma generation chamber 11 is provided with a high-frequency power supply 14 for supplying a high-frequency electric power at 13.56 MHz and with antennas 12 for discharging the high-frequency electric power supplied from the high-frequency power supply 14, the chamber 11 being partitioned from the exterior by a partition wall of a bell jar type. The cylindrical portion of the partition wall is of 95mm inner diameter.

[0034] Between the high-frequency power supply 14 and the antennas 12 there intervenes a matching circuit 13 for impedance matching. The high-frequency electric power discharged from the antennas 12 serves to transform an conduction type impurity containing gas within the plasma generation chamber 11 into a helicon plasma. The conduction type impurity containing gas used herein is a gas filling the plasma generation chamber 11 as a result of supply thereof through gas inlets 18 of the plasma flow passage/shaping chamber 16 which will be described later.

[0035] The plasma flow passage/shaping chamber 16 is provided with the gas inlets 18 for the gas containing conduction type impurities (hereinafter, may be referred to simply as impurities) which impart a conduction type to the semiconductor substrate and vary the resistivity of the semiconductor substrate. Available as the conduction type impurity containing gas is a diboron gas containing boron which imparts a conduction type of p-type (hereinafter, may be referred to simply as p-type) to silicon and varies the resistivity, or similarly a gallium hydrogen compound gas or a gallium organometallic compound gas. Alternatively, there may be also used a phosphine gas containing phosphorus which imparts a conduction type of n-type (hereinafter, may be referred to simply as n-type) to silicon and varies the resistivity, or similarly an arsenic hydrogen compound gas or an arsenic organometallic compound gas.

[0036] The plasma flow passage/shaping chamber 16 is interposed between the plasma generation chamber 11 and the impurity introduction chamber 19, the chamber 16 providing a flow passage through which helicon plasma is fed from the plasma generation chamber 11 into the impurity introduction chamber 19. The interior of the plasma flow passage/shaping chamber 16 is hermetically defined by a cylindrical partition wall having an inner diameter of approx. 350 mm.

[0037] In the meantime, high-density plasmas such as the helicon plasma interact strongly with the internal walls of the system, with the result that useful plasmas may somewhat be lost by the interaction. To avoid this, the partition wall of the plasma flow passage/shaping chamber 16 is provided at its outer periphery with permanent magnets (magnetic field generation means) 17 for generating a cusped magnetic field to restrict the extent of the helicon plasma flowing through the plasma flow passage/shaping chamber 16 to thereby complete its distribution form. The cusped magnetic field serves to suppress the extent of the helicon plasma flowing through the interior of the plasma flow passage/shaping chamber 16 to complete its distribution form.

[0038] Referring to Fig. 2 and particularly to Fig. 5, the arrangement of the permanent magnets 17 is depicted. The permanent magnets 17 are arranged circumferentially along the outer periphery of the partition wall of the

plasma flow passage/shaping chamber 16 in such a manner that N-poles and S-poles alternate. Eight circumferential arrays each consisting of such a series of permanent magnets along the periphery are arranged one upon another in the height direction.

[0039] As illustrated in Fig. 5, magnetic fields are generated principally between the adjacent permanent magnets 17 and become prevailing in the interior of the plasma flow passage/shaping chamber 16. Adjustment may be made of the magnetic field strength of each permanent magnet 17 and of the interval between the adjacent N-poles and S-poles so as to be able to delimit the space in which plasma is present depending on the diameter of the semiconductor substrate 100.

[0040] Fig. 6 illustrates a distribution of the magnetic field strength measured in the radial direction from the inner wall surface of the partition wall of the plasma flow passage/shaping chamber 16 toward the center of the plasma flow passage/shaping chamber 16. In Fig. 6, the axis of abscissas represents the distance r (mm) from the partition wall toward the center and the axis of ordinates represents the strength of magnetic field (gauss).

[0041] As can be seen in the graphic representation, the strength of magnetic field becomes substantially null at locations approx. 60 mm or farther apart from the inner wall surface of the partition wall. Thus, the helicon plasma passing through the plasma flow passage/shaping chamber 16 is present or confined mainly within the diameter of 230 mm and is prevented from spreading outward therefrom. It is thus possible to prevent any possible dispersion of plasma to achieve an enhanced uniformity in the distribution of plasma density, as well as to prevent any possible loss of plasma within the plasma flow passage/shaping chamber 16 and within the impurity introduction chamber 19 to improve the efficiency.

[0042] Fig. 7 is a diagram schematically showing the distribution of plasma density within the plasma flow passage/shaping chamber 16 under such a cusped magnetic field. Fig. 8 is a graphic representation showing the result of measurement of the distribution of plasma passing through the interior of the chamber 16 under the cusped magnetic field. In Fig. 8, the axis of abscissas represents the position (cm) within the chamber 16 and the axis of ordinates represents the ion saturation current density (mA/cm^2).

[0043] Plasma is generated in the condition that Ar gas pressure is 3 mTorr with the plasma generation power of 2 kW. The ion saturation current density was measured by use of a fast probe 33 manufactured by PMT (Plasma & Materials Incorporation) and disposed on the outside of the partition wall of the plasma flow passage/shaping chamber 16 as shown in Fig. 7. The result of measurement of Fig. 8 shows a highly improved uniformity in the plasma distribution.

[0044] Furthermore, in the plasma flow passage/shaping chamber 16, a diborane or other gas may possibly adhere to the inner wall surfaces of the partition wall, which would require a cumbersome periodical cleaning of the inner wall surfaces of the partition wall. To avoid this, a quartz made protection wall 16a is provided along the inner wall surfaces of the partition wall. Thus, the conduction type impurities in plasma state will adhere to this protection wall 16a, so that the conduction type impurities are prevented from directly adhering on the inner wall surfaces of the partition wall. The inner surfaces of the protection wall 16a are abraded down to a surface roughness of the order of 10μ m to provide as small a wall surface as possible in order to prevent any adhesion of metal contaminant or degassing.

[0045] Then, the impurity introduction chamber 19 is partitioned from the exterior by a tubular partition wall having the same inner diameter as that of the plasma flow passage/shaping chamber 16, the chamber 19 being provided with a substrate holding fixture 20 for retaining the semiconductor substrate 100. The exhaust device 28 is connected via a throttle valve 27 to the impurity introduction chamber 19. This exhaust device 28 serves to reduce the pressure not only within the impurity introduction chamber 19 but also within the plasma flow passage/shaping chamber 16 and the plasma generation chamber 11. This chamber 19 allows helicon plasma of the conduction type impurity containing gas to come into contact with the semiconductor substrate 100, to thereby introduce the conduction type impurities into the semiconductor substrate 100.

[0046] Unlike the plasma flow passage/shaping chamber 16, no magnets are disposed around the outer periphery of the partition wall of the impurity introduction chamber 19. A withdrawal port 21a is also provided for withdrawing the substrate holding fixture 20 from the impurity introduction chamber 19 for the purpose of cleaning or the like. The draw-out port 21a is usually hermetically sealed by a sealing door 21. This draw-out port 21 is utilized to connect an electric power supply wiring 24 from a bias power supply part 23 through the interior of a retaining arm 25 of the substrate holding fixture 20 to a bias applying electrode of the substrate holding fixture 20.

[0047] On the other hand, the impurity introduction chamber 19 is also provided with a quartz made protection wall 19a for covering the inner wall surfaces of the partition wall in the same manner as the plasma flow passage/shaping chamber 16. An impurity gas in plasma state adheres to the protection wall 19a to thereby prevent any adhesion of the impurity gas to the inner wall surfaces of the partition wall. Similarly, the inner wall surfaces of the protection wall 19a are abraded down to a surface roughness of the order of 10μ m in order to prevent any adhesion of metal contaminants or degassing.

[0048] The upper and lower protection walls 16a and 19a may be dismounted in order to remove any impurities adhered to the upper protection wall 16a of the plasma flow passage/shaping chamber 16 or to the lower protection wall 19a of the impurity introduction chamber 19, after doping to the semiconductor substrate 100 by

use of the plasma doping system described above. In such a case, the lower protection wall 19a is first drawn out of the impurity introduction chamber 19 in the lateral direction. and thereafter the upper protection wall 16a is pulled down to the impurity introduction chamber 19 and then similarly drawn out of the impurity introduction chamber 19 in the lateral direction.

[0049] Referring then to Fig. 4, a detail structure is illustrated of the substrate holding fixture 20 provided on the impurity introduction chamber 19.

[0050] The substrate holding fixture 20 has the outermost part formed from an insulator 46 of alumina. An electrode 43 for electrostatic suction is embedded so that the semiconductor substrate 100 is electrostatically retained by electrostatic chuck. A heater is provided for use as heating means (temperature regulation means) 45 at the lower portion of the electrode 43 for electrostatic suction. At the bottom of the electrode 43 for electrostatic suction there is provided a piping through which a coolant such as, e.g., helium gas flows, the piping being used as cooling means (temperature regulation means) 42. Reference numeral 44 denotes an electrode for grounding.

[0051] In case the semiconductor substrate 100 has a formed thereon resist film acting as a mask for selective introduction of conduction type impurities, the semiconductor substrate 100 is cooled by the cooling means 42 in order to prevent any change in quality of the resist film when the temperature of the semiconductor substrate 100 rises as a result of exposure to plasma. Instead, in case no resist film is used, the semiconductor substrate 100 may be heated by the heating means 45 when the semiconductor substrate 100 and the plasma are in contact with each other, to thereby activate the impurities simultaneously with the introduction of the impurities.

[0052] The substrate holding fixture 20 is further provided with a built-in bias applying electrode 41 coupled to an AC power source 26 for supplying AC power at approx. 100 kHz as shown in Fig. 2. The DC or AC power is fed in a continuous or intermittent (pulse-like) manner to apply a bias voltage to the semiconductor substrate 100. This gives rise to a potential difference between the plasma and the semiconductor substrate 100 whereupon impurity ions can be accelerated by the resultant electric field so as to be introduced into the semiconductor substrate 100. As a result, a wider range is imparted to the regulation of the depth of introduction of the impurities. In Fig 2, reference numeral 23 denotes the bias power supply part, with the output end of the AC power source 26 being connected on one hand via a low-pass filter 61 to a voltage measurement device 62. The output end of the AC power source 26 is connected on the other by the wiring 24 to the electrode 41 of the substrate holding fixture 20.

[0053] Although the AC power source 26 is used as the bias power supply source in Fig. 2, the AC power source 26 may be replaced by a DC power source for supplying DC power. In such a case, the voltage measurement device 62 may directly be connected to the output end of the AC power source 26, with the omission of the capacitor and the low-pass filter 61 coupled to the output end of the AC power source 26.

[0054] Furthermore, the substrate holding fixture 20 may be secured to a rotary shaft perpendicular to the substrate retaining surface so that it can rotate around the shaft. This will contribute to an improved uniformity of distribution of the impurities introduced.

[0055] Description will then be made of a method of selectively introducing impurities into the semiconductor substrate 100 by use of the above plasma doping system. Figs. 9A to 9D are cross-sectional views illustrated in the process sequence.

[0056] First, as shown in Fig. 9A, a resist film (photosensitive etching-proof film) 51 having openings 52 is formed on the surface of an n-type silicon semiconductor substrate 100. The openings 52 are formed in regions into which impurities are to be introduced. After loading of this semiconductor substrate 100 into the load-lock chamber 102, reduced pressures are given to the interiors of the transfer chamber 101, load-lock chamber 102, impurity introduction chamber 19, ashing chamber 104 and annealing chamber 105. After a predetermined pressure has been reached, the semiconductor substrate 100 is conveyed from the load-lock chamber 102 to the interior of the transfer chamber 101.

[0057] The semiconductor substrate 100 is then conveyed from the interior of the transfer chamber 101 into the impurity introduction chamber 19. Subsequently, an conduction type impurity containing gas, e.g., diborane gas containing boron for imparting p-type conductivity to the silicon layer is fed through the gas inlets 18 of the plasma flow passage/shaping chamber 16 into the plasma generation chamber 11. A high-frequency power is then supplied from the high-frequency power source 14 and is discharged from the antennas 12. This transforms the conduction type impurity containing gas into plasma, allowing a generation of helicon plasma having a plasma density of 10^{18} to 10^{19} cm^{-3}.

[0058] The helicon plasma then flows toward the downstream impurity introduction chamber 19. At that time, within the plasma flow passage/shaping chamber 16 there is generated a cusped magnetic field, which restrains the helicon plasma from diffusing toward its peripheral portions, allowing the helicon plasma to flow along the longitudinal axis of the plasma flow passage/shaping chamber 16. Thus, due to the suppression of extinction of plasma impinging on the inner wall surfaces of the partition wall, the loss of plasma in motion becomes extremely reduced.

[0059] Then, as shown in Fig. 9B, the plasma of the conduction type impurities comes into contact with the semiconductor substrate 100 placed within the impurity introduction chamber 19 so that the conduction type impurities are introduced into the semiconductor substrate 100 to form impurity introduction regions 53 therein. De-

pending on the cases, the depth of introduction or the like may be regulated by previously applying a bias to the substrate holding fixture 20 by use of the AC power source 26 or the DC power source.

[0060] The semiconductor substrate 100 is then withdrawn from the impurity introduction chamber 19 and is conveyed to the transfer chamber 101 prior to conveyance to the interior of the ashing chamber 104.

[0061] Oxygen gas is then led into the ashing chamber 104 for being transformed into plasma. The resultant oxygen plasma comes into contact with the resist film 51 to chemically etch the latter. After the complete removal of the resist film 51, the semiconductor substrate 100 is withdrawn from the ashing chamber 104 and is conveyed to the annealing chamber 105.

[0062] The semiconductor substrate 100 is then heated for ten sec. at 950°C in an atmosphere of nitrogen, to activate the conduction type impurities which are present within the semiconductor substrate 100. p-type regions 53a are thereby formed to complete a series of steps related to the plasma doping.

[0063] The semiconductor substrate 100 is thereafter withdrawn from the annealing chamber 105 and is conveyed to the interior of the transfer chamber 101, which in turn is followed by the conveyance from the transfer chamber 101 to the interior of the load-lock chamber 102.

[0064] Afterward, the pressure within the load-lock chamber 102 is returned to the atmospheric pressure, and then the semiconductor substrate 100 is unloaded from the load-lock chamber 102.

[0065] According to the plasma doping system of the embodiment of the present invention as set forth hereinabove, even when the semiconductor substrate (wafer) has an enlarged diameter, there is no need for too a large-sized high-frequency power source 14 due to its low frequency as of 13.56 MHz. A simple structure of the antennas 12 will also eliminate a need for the antennas to have even larger dimensions. In view of its applications, compact ones such as permanent magnets 17 can be used as the magnetic field generation means 17 disposed on the plasma flow passage within the plasma flow passage/shaping chamber 16, thereby enabling the increase in size to be suppressed.

[0066] It is therefore possible for the doping system using the helicon plasma in accordance with the present invention to reduce the floor areas required for the placement of the system as compared with the conventional doping system using the ECR plasma.

[0067] Furthermore, communications are established via a single transfer chamber 101 among the impurity introduction chamber 19 of the plasma doping part 103, the ashing chamber 104 and the annealing chamber 105, whereby a single system can perform a series of process steps related to the plasma doping such as introduction of conduction type impurities, removal of the resist mask for the selective introduction of the conduction type impurities and activation of the conduction type impurities.

[0068] By the way, in the case of individually placing each apparatus, it requires a working space for the workers in addition to the net floor area for the space of placement of each apparatus. On the contrary, this embodiment integrates those apparatuses into a single system as described above, thereby making it possible to reduce the working spaces. It is therefore possible for the thus integrated plasma doping system to reduce the floor area necessary for the placement of the system, as compared with the case of individual placement of each apparatus.

[0069] Although the present invention has been described in detail based on the embodiment thereof, it will be appreciated that the scope of present invention is not limited to the example specifically shown in the above embodiment but that it covers all variants of the above embodiment insofar as it does not depart from the sprit of the present invention.

[0070] In the above embodiment, for example, the present invention has been applied to the plasma doping system obtained by integrating into a single system the plasma doping part 103, the ashing chamber 104 for removing the resist film 51 and the annealing chamber 105 for activating the impurities introduced into the semiconductor substrate 100, but this is in no way restrictive. The present invention could be applied to the system consisting only of the plasma doping part 103.

[0071] The plasma flow passage/shaping chamber 16 and the impurity introduction chamber 19 have been provided with the partition walls having inner wall surfaces protected by the quartz made protection walls 16a and 19a, but the protection walls may be made of aluminium or ceramics.

[0072] Although the plasma doping system of the present invention has employed the helicon plasma as plasma source, use may be made of ICP (Inductive Coupled Plasma), multi-spiral coil (MSC) ICP, magnetron two-frequency plasma, triode plasma, LEP (Lissajou electron Plasma), etc. All of the above are well known as the plasma sources for etching systems, with the use of high-frequency electric power of the order of 1 to 20 MHz.

[0073] Furthermore, the conduction type impurity gas inlets 18 have been provided in the plasma flow passage/shaping chamber 16, but it may be provided in the plasma generation chamber 11.

[0074] As set forth hereinabove, the plasma doping system of the present invention is provided with the high-frequency power source which supplies high-frequency electric power for generating the helicon plasma of the conduction type impurity containing gas and with the antennas for discharging the high-frequency electric power, whereby it is possible to suppress an increase in dimensions of the high-frequency power source and the antennas even in the event of enlarged wafer diameters. It is also possible to suppress an increase in dimensions of the magnetic field generation means pro-

vided in the plasma flow passage/shaping chamber acting as the flow passage for the helicon plasma.

[0075] As a result, the doping system using the helicon plasma of the present invention is able to reduce the floor area required for the placement of the system as compared with the doping system using the ECR plasma.

[0076] By virtue of the juxtaposed junction to a single transfer chamber of the plasma introduction chamber, the mask removal chamber and the annealing chamber of the plasma doping system, a single system is capable of performing a series of process steps related to the plasma doping such as introduction of conduction type impurities, the removal of the resist mask for the selective introduction of the conduction type impurities, and the activation of the conduction type impurities.

[0077] This achieves a reduction in the floor area required for the placement of the system as compared with the case of individual placement of each apparatus.

Claims

1. A plasma doping system comprising:

    a plasma generation chamber (11) provided with a high-frequency power source (14) for supplying a high-frequency electric power and with antennas (12) for discharging the high-frequency electric power, said plasma generation chamber (11) serving to generate a helicon plasma of a gas containing conduction type impurities which impart a conduction type to a semiconductor substrate (100) and which vary the resistivity of said semiconductor substrate (100), by use of the high-frequency electric power discharged from said antennas (12);
    an impurity introduction chamber (19) provided with a substrate holding fixture (20) and for causing said helicon plasma of said conduction type impurity containing gas to come into contact with said semiconductor substrate (100) to thereby introduce said conduction type impurities into said semiconductor substrate (100); and
    a plasma flow passage/shaping chamber (16) interposed between said plasma generation chamber (11) and said impurity introduction chamber (19) and providing a flow passage through which said helicon plasma flows from said plasma generation chamber (11) to said impurity introduction chamber (19), said plasma flow passage/shaping chamber (16) being provided with magnetic field generation means (17) for generating a magnetic field to restrict the extent of said helicon plasma flowing through said flow passage.

2. A plasma doping system according to claim 1, wherein either said plasma generation chamber (11) or said impurity introduction chamber (19) is provided with inlets (18) for said conduction type impurity containing gas.

3. A plasma doping system according to claim 1, wherein said substrate holding fixture (20) is connected to a DC power source (62) or an AC power source (26) which supplies an electric power for applying a bias voltage to said semiconductor substrate (100) retained by said substrate holding fixture.

4. A plasma doping system according to claim 1, further comprising temperature regulation means (42,45) for cooling said semiconductor substrate (100) retained by said substrate holding fixture (20) or for heating the same.

5. A plasma doping system according to claim 1, further comprising rotationally driving means for rotating said substrate holding fixture (20) around a rotational axis substantially orthogonal to the surface of said substrate holding fixture (20) retaining said semiconductor substrate (100).

6. A plasma doping system according to claim 1, further comprising a mask removal chamber (104) for removing a mask which is formed on a surface of said semiconductor substrate (100) and which allows a selective introduction of said conduction type impurities into said semiconductor substrate (100); an annealing chamber (105) for raising the temperature of said semiconductor substrate (100) to thereby activate said conduction type impurities which are present within said semiconductor substrate (100), and a transfer chamber (101), wherein said impurity introduction chamber (19), said mask removal chamber (104) and said annealing chamber (105) are joined separately to said transfer chamber (101) in a juxtaposed manner.

7. A plasma doping method for introducing said conduction type impurities into said semiconductor substrate (100) by use of a plasma doping system according to claim 1, said method comprising the steps of:

    leading said conduction type impurity containing gas into said plasma generation chamber (11);
    discharging said high-frequency electric power from said antennas (12) to thereby generate a helicon plasma of said gas containing said conduction type impurities;
    leading said helicon plasma through said plasma flow passage/shaping chamber (16) into

said impurity introduction chamber (19) under the presence of a magnetic field generated by said magnetic field generation means (17); and causing said helicon plasma to come into contact with said semiconductor substrate (100) in said impurity introduction chamber (19) to thereby introduce said impurities into said semiconductor substrate (100).

8. A plasma doping method for selectively introducing said conduction type impurities into said semiconductor substrate (100) having a formed thereon photosensitive etching-proof mask by use of said plasma doping system according to claim 6, said method comprising the steps of:

conveying said semiconductor substrate (100) into a load-lock chamber (102) to thereafter convey the same through said transfer chamber (101) into said impurity introduction chamber (19);
leading said conduction type impurity containing gas into said plasma generation chamber (11);
discharging said high-frequency electric power from said antennas (12) to thereby generate a helicon plasma of said conduction type impurity containing gas;
leading said helicon plasma through said plasma flow passage/shaping chamber (16) into said impurity introduction chamber (19) under the presence of a magnetic field generated by said magnetic field generation means (17);
causing said helicon plasma to come into contact with said semiconductor substrate (100) to thereby selectively introduce said impurities into said semiconductor substrate (100) in conformity with said photosensitive etching-proof mask;
conveying said semiconductor substrate (100) from said impurity introduction chamber (19) through said transfer chamber (101) into said mask removal chamber (104), to thereat remove said photosensitive etching-proof mask lying on said semiconductor substrate (100); and
conveying said semiconductor substrate (100) from said mask removal chamber (104) through said transfer chamber (101) into said annealing chamber (105), to thereat heat said semiconductor substrate (100) to activate said conduction type impurities introduced into said semiconductor substrate (100).

9. A plasma doping method according to claim 7 or 8, wherein electrical conductivity is possessed by partition walls for separating said impurity introduction chamber (19) from the exterior, while DC power or AC power is applied to said semiconductor substrate (100) so as to generate a bias voltage in said substrate (100) and then said conduction type impurities are introduced into said semiconductor substrate (100) by use of the resultant potential difference occurring between said semiconductor substrate (100) and said helicon plasma.

10. A plasma doping method according to claim 7 or 8, wherein said semiconductor substrate (100) is cooled or heated upon the introduction of said conduction type impurities into said semiconductor substrate (100).

Fig. 1

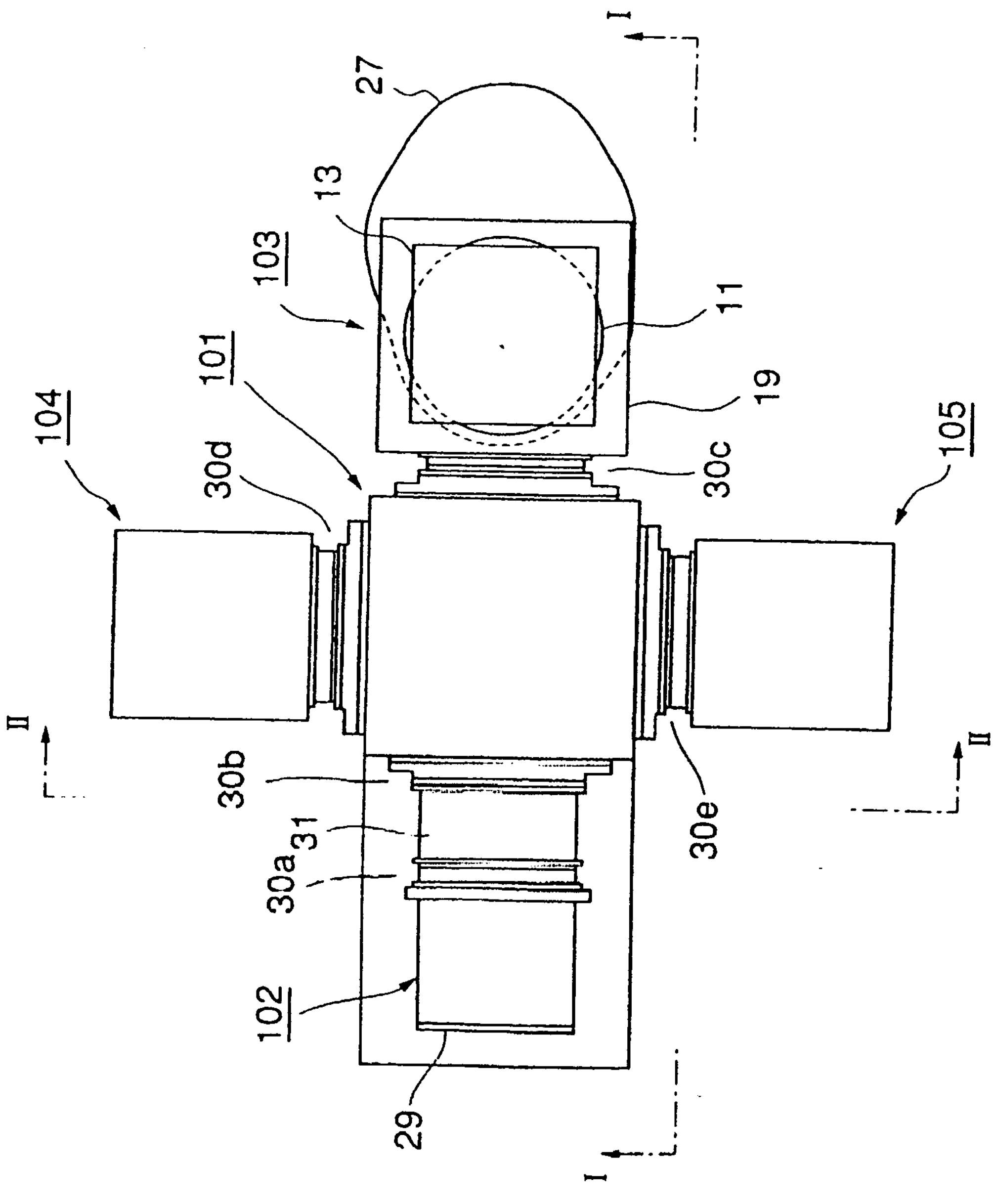


Fig. 2

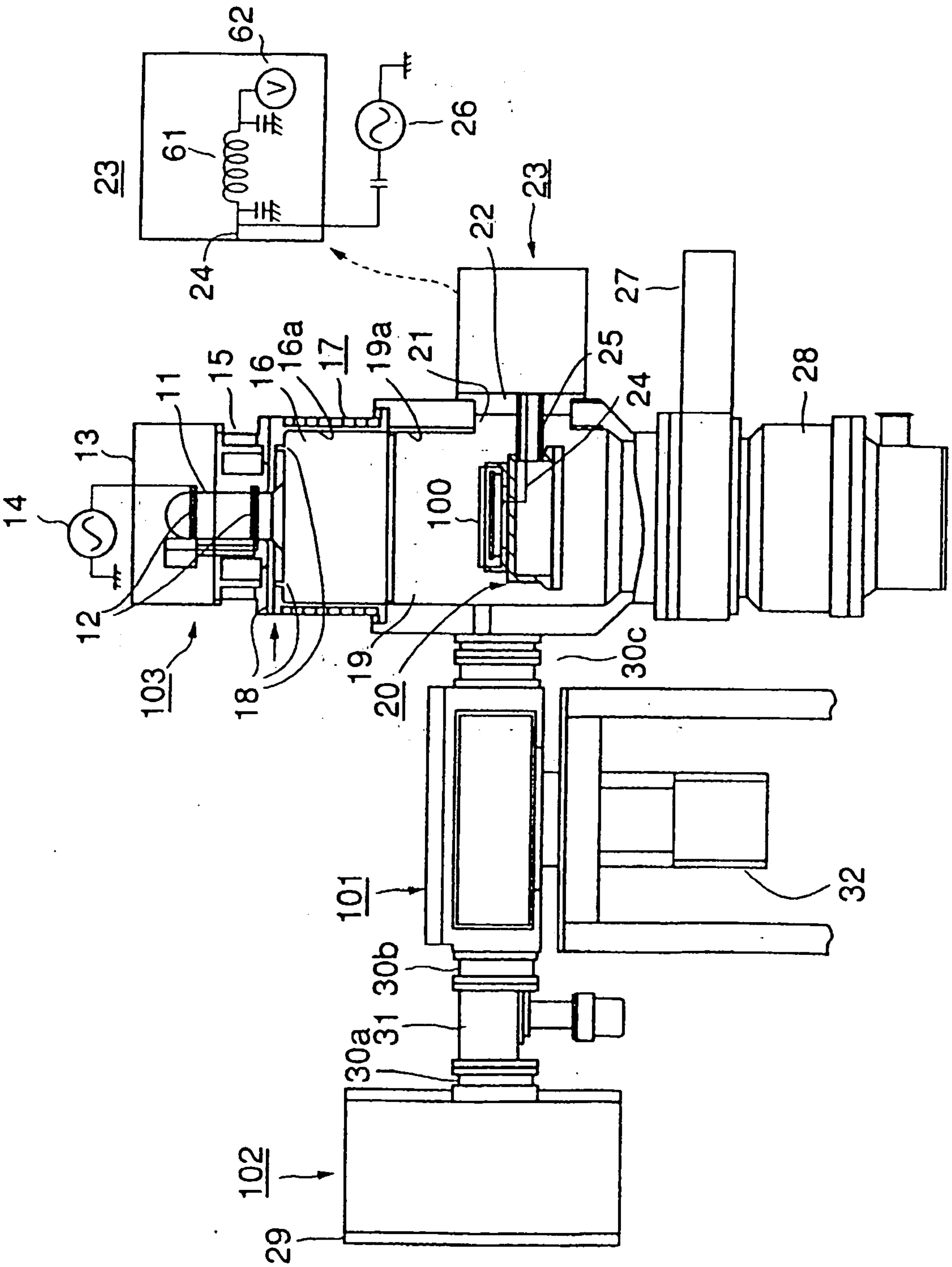

62
V
61
23
26
24
22
23
27
11
15
16
16a
17
19a
21
25
24
28
13
14
100
12
103
18
19
20
30c
101
32
30b
31
30a
102
29

Fig. 3

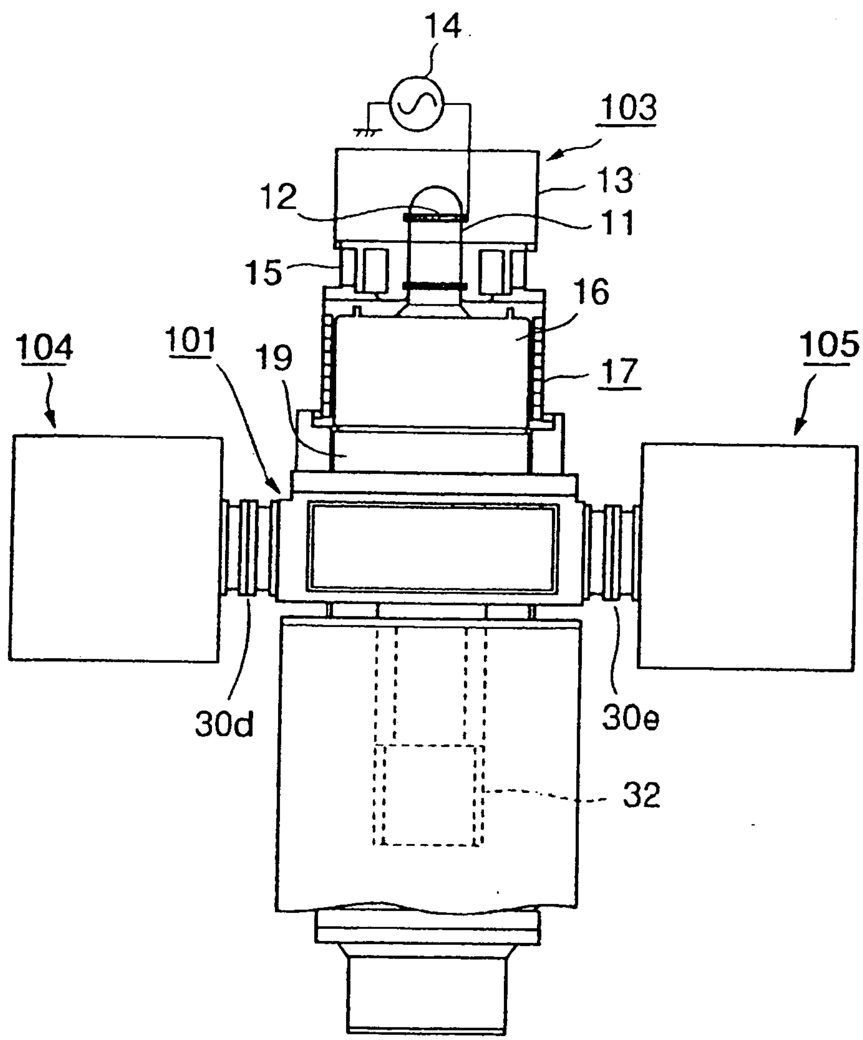


Fig. 4

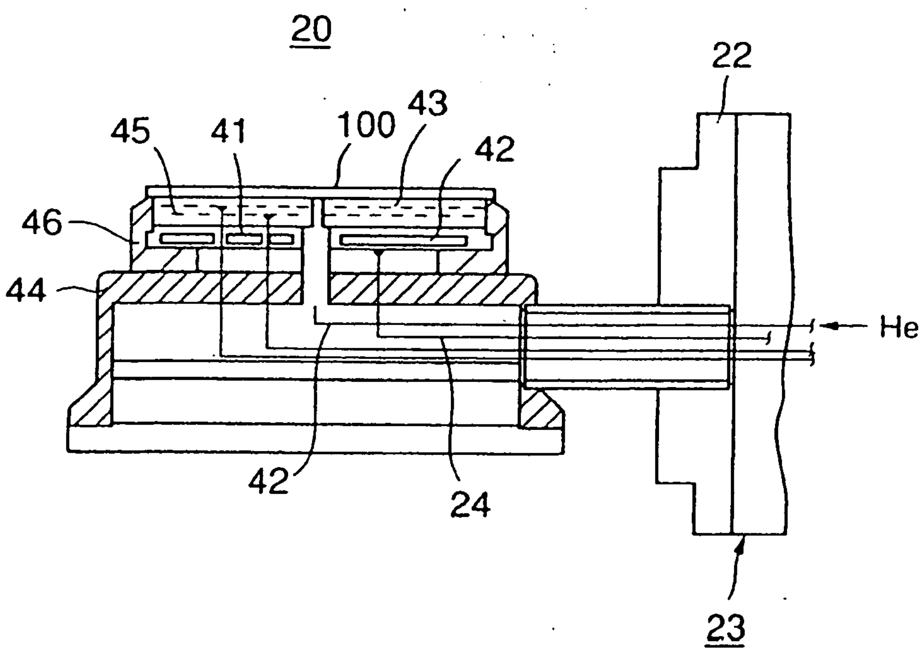


Fig. 5

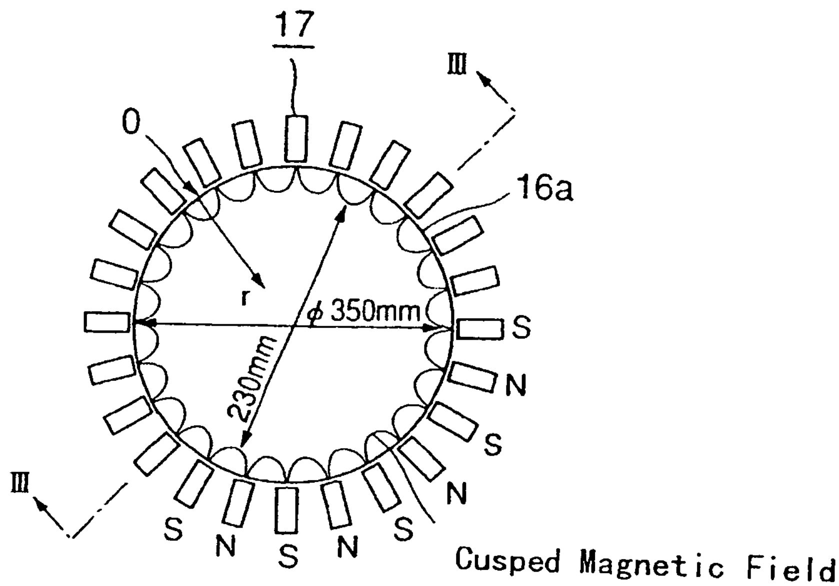

17
0
Ⅲ
16a
r
φ 350mm
230mm
S
N
S
N
Ⅲ
S
N
S
N
S
Cusped Magnetic Field

Fig. 6

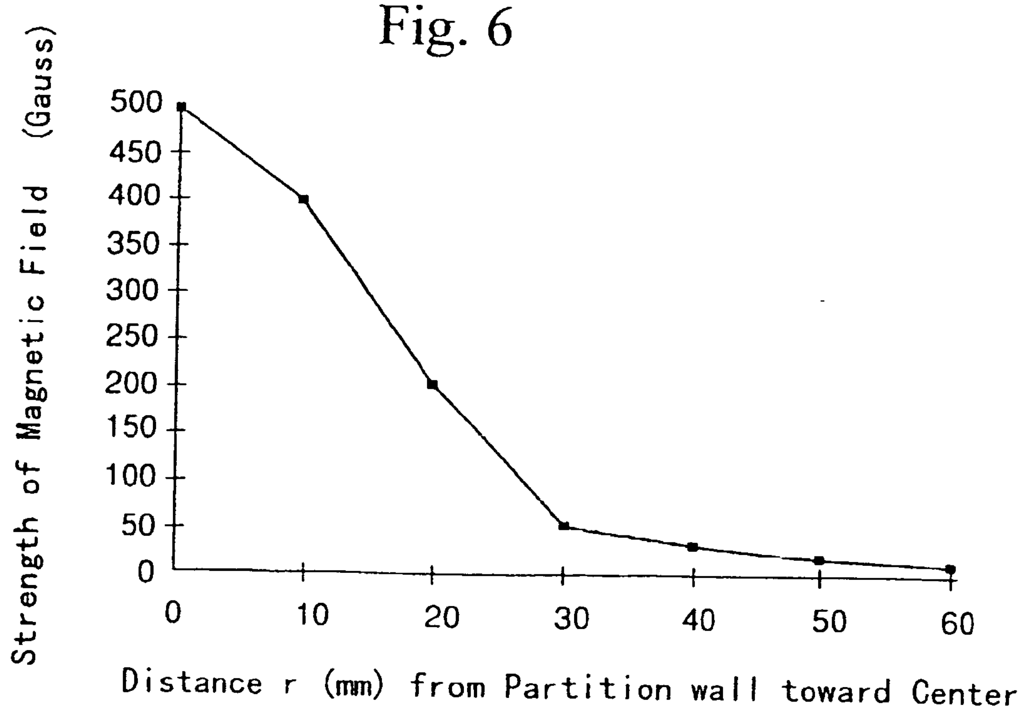

Strength of Magnetic Field (Gauss)
500
450
400
350
300
250
200
150
100
50
0
0
10
20
30
40
50
60
Distance r (mm) from Partition wall toward Center

Fig. 7

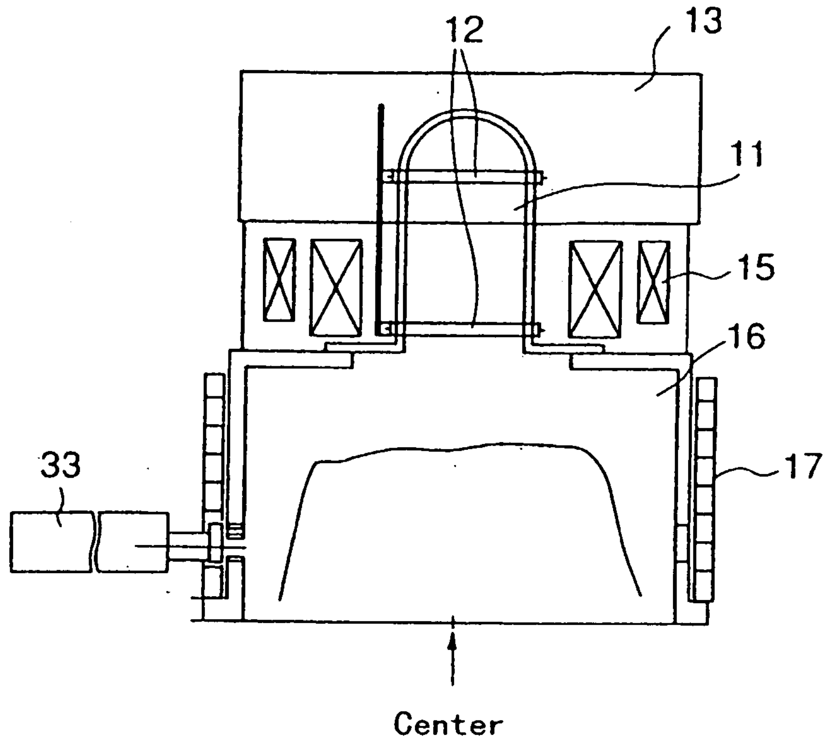

12
13
11
15
16
33
17
Center

Fig. 8

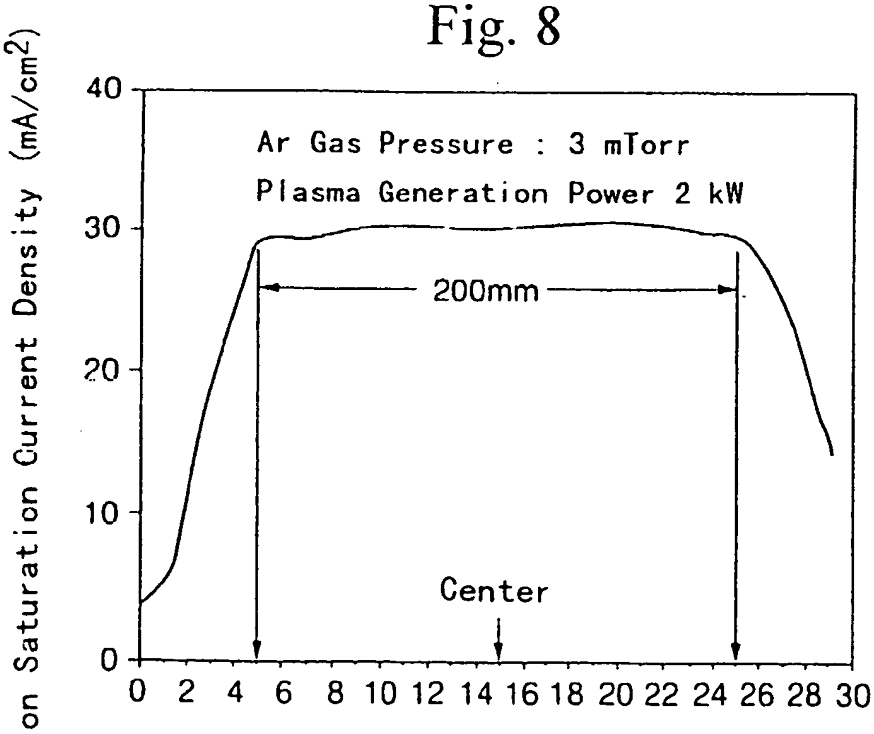

Ion Saturation Current Density (mA/cm2)
Ar Gas Pressure : 3 mTorr
Plasma Generation Power 2 kW
200mm
Center
0
10
20
30
40
0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30

Fig. 9A

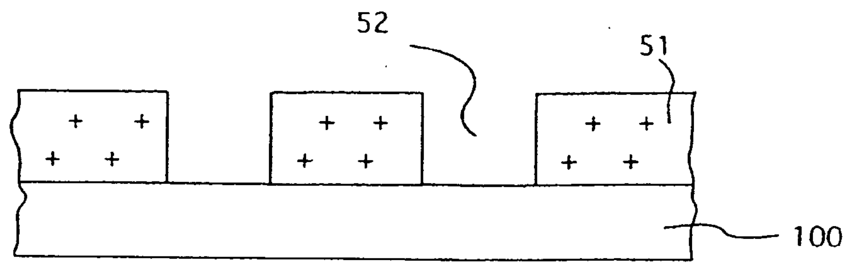


Fig. 9B

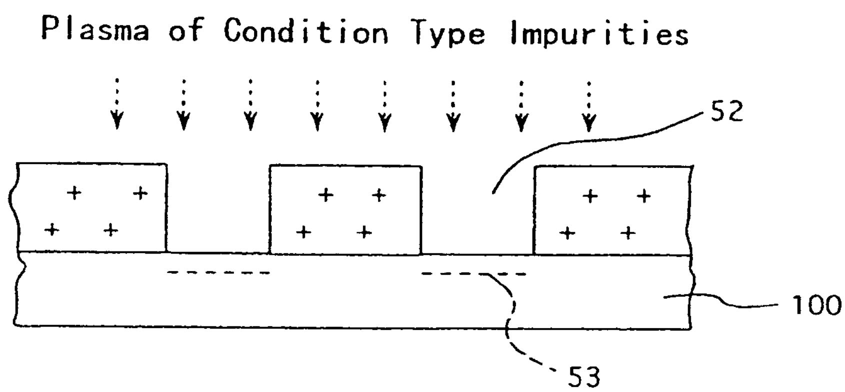


Fig. 9C

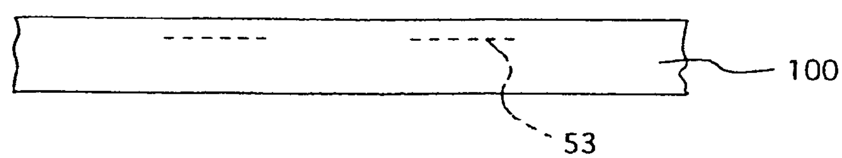
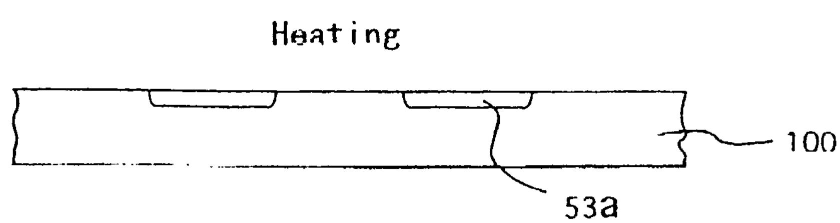


Fig. 9D



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 12 1909

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	EP 0 665 307 A (CANON SALES CO INC ;ALCAN TECH CO INC (JP); SEMICONDUCTOR PROCESS) 2 August 1995 (1995-08-02) * abstract * * column 14, line 9-15 * * figure 1 * ---	1-9	H01J37/32
A	EP 0 489 407 A (APPLIED MATERIALS INC) 10 June 1992 (1992-06-10) * abstract * * page 15, line 1-30 * * figure 1 * ---	1-9	
A	EP 0 570 484 A (PLASMA & MATERIALS TECH) 24 November 1993 (1993-11-24) * abstract * * figures 2-6 * -----	1-9	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	31 August 2000	Winkelman, A

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31-08-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0665307 A	02-08-1995	JP 7111261 A	25-04-1995
EP 0489407 A	10-06-1992	JP 2519364 B	31-07-1996
		JP 4290428 A	15-10-1992
		US 5556501 A	17-09-1996
		US 5707486 A	13-01-1998
		US 6068784 A	30-05-2000
EP 0570484 A	24-11-1993	US 5122251 A	16-06-1992
		DE 69218924 D	15-05-1997
		DE 69218924 T	15-01-1998
		JP 6506084 T	07-07-1994
		AT 151569 T	15-04-1997
		AU 1352192 A	07-09-1992
		ES 2102497 T	01-08-1997
		WO 9214258 A	20-08-1992
		US 5421891 A	06-06-1995
		US 5429070 A	04-07-1995

EPO FORM P0459

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